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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/826,921

04/16/2004

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1890-0079

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7590

02/09/2006

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EXAMINER

DIAZ, JOSE R

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/826,921

Applicant(s)

TADDIKEN, HANS

Examiner

José R. Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-7,10-13 and 18-20 is/are rejected.
- 7) ☒ Claim(s) 3,11 and 15-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/12/04
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of claims 1-7 and 10-20 in the reply filed on January 26, 2005 is acknowledged.

### ***Priority***

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Germany on October 17, 2001. It is noted, however, that applicant has not filed a certified copy of the DE 10 151 202.3 application as required by 35 U.S.C. 119(b).

### ***Drawings***

3. The drawings are objected to because figure 1 is confusing since the regions cannot be properly identified. In addition, applicant fails to label all regions shown in figure 1 (i.e. floating region, the blank space between region 112 and substrate100, etc). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

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changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-7, 10, 12-14, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Rumennik et al. (US Pat. No. 6,207,994 B1).

Regarding claim 1, Rumennik et al. teaches a semiconductor structure, comprising:

a substrate (16) [see fig. 1];

a source area (13, 14, 15) formed in the substrate [see fig. 1];

a drain area (19,24,25) formed in the substrate and comprising a doping of a first conductivity type (N-type) [see fig. 1], wherein the drain area comprises:

a first drain portion (19) having a first doping concentration (N+), and

a second drain portion (24) having a second doping concentration (N),

wherein the first doping concentration (N+) is higher than the second doping concentration (N),

wherein the second drain portion (24) includes a first region (18) comprising a doping of a second conductivity type (P-type) which is different to the first conductivity type [see fig. 1];

a second region (25) formed in the substrate below the second drain portion and comprising a doping of first conductivity type (N-type) [see fig. 1]; and

a channel area (28) the substrate between the source area and the second drain portion [see fig. 1].

Regarding claim 2, Rumennik et al. teaches that the second region (25) in the substrate is formed such that the second region (25) is substantially opposite to the first region (18) in the second drain portion [see fig. 1].

Regarding claim 4, Rumennik et al. teaches that the first region (18) is embedded in the second drain portion (24) [see fig. 1].

Regarding claim 5, Rumennik et al. teaches that the first region (18) is formed in the second drain portion (24) such that the first region is exposed at a surface of the substrate [see col. 5, lines 1-5 and region 60 in fig. 4].

Regarding claim 6, Rumennik et al. teaches that the first region (18) is floating [see fig. 1].

Regarding claim 7, Rumennik et al. teaches that the first region (18) is connected to a reference potential [see col. 5, lines 1-5].

Regarding claim 10, Rumennik et al. teaches that a semiconductor comprising:

a substrate (16) [see fig. 1];

a source area (14) formed in the substrate and having a doping of a first conductivity type (N+) [see fig. 1];

a drain area (19, 24) formed in the substrate and displaced from the source area (14) [see fig. 1], the drain area comprising:

a first drain portion (19) having a doping of the first conductivity type and a first doping concentration (N+), and

a second drain portion (24) having a doping of the first conductivity type and a second doping concentration (N) lower than the first doping concentration (N+) [see fig. 1], the second drain portion (1) being disposed between the first drain portion (19) and the source area (14) [see fig. 1];

a first region (18) formed in the second drain region (24), the first region having a doping of a second conductivity type (P-type) which is different than the first conductivity type [see fig. 1];

a second region (25) formed below the second drain region and having a doping of the first conductivity type (N-type) [see fig. 1]; and

a channel area (28) in the substrate between the source area and the drain area [see fig. 1].

Regarding claim 12, Rumennik et al. teaches the second region (25) disposed substantially below the first region (18) in the substrate [see fig. 1].

Regarding claim 13, Rumennik et al. teaches that the second region (25) does not extend below the channel area (28) [see fig. 1].

Regarding claim 14, Rumennik et al. teaches a gate structure (12) formed on a surface of the substrate above the channel (28) and wherein the second drain portion (25) does not extend substantially below the gate structure (12) [see fig. 1].

Regarding claim 18, Rumennik et al. teaches the first region (18) and the second region (25) form an area of dual implantation [see fig. 1].

Regarding claim 19, Rumennik et al. teaches that the depth and doping concentration of the second region (25) compensates for the increased resistance resulting in the second drain portion (24) resulting from the depth and doping concentration of first region (18) disposed therein [see col. 4, lines 36-40, 45-51, 61-67 and col. 6, lines 10-18].

Regarding claim 20, Rumennik et al. teaches the second drain region is flat region (18) and the second region (25) form an area of dual implantation [see fig. 1].

6. Claims 1-2, 4-5, 7, 10, 12 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Onishi et al. (US Pat. No. 6,756,636 B2).

Regarding claim 1, Onishi et al. teaches a semiconductor structure, comprising:  
a substrate [consider the substrate formed by layers 4 and 5 in fig. 2];  
a source area (7) formed in the substrate [see fig. 2];  
a drain area (1,2,8) formed in the substrate and comprising a doping of a first conductivity type (N-type) [see fig. 2], wherein the drain area comprises:

    a first drain portion (8) having a first doping concentration (N+), and  
    a second drain portion (1) having a second doping concentration (N),  
    wherein the first doping concentration (N+) is higher than the second doping concentration (N),

    wherein the second drain portion (1) includes a first region (2) comprising a doping of a second conductivity type (P-type) which is different to the first conductivity type [see fig. 2];  
    a second region (4) formed in the substrate below the second drain portion and comprising a doping of first conductivity type (N-type) [see fig. 2]; and  
    a channel area (3) the substrate between the source area and the second drain portion [see fig. 2].

Regarding claim 2, Onishi et al. teaches that the second region (4) in the substrate is formed such that the second region (4) is substantially opposite to the first region (2) in the second drain portion [see fig. 2].

Regarding claim 4, Onishi et al. teaches that the first region (2) is embedded in the second drain portion (1) [see fig. 2].



Regarding claim 5, Onishi et al. teaches that the first region (2) is formed in the second drain portion (1) such that the first region is exposed at a surface of the substrate [see fig. 2].

Regarding claim 7, Onishi et al. teaches that the first region (2) is connected to a reference potential through gate electrode 9 and electrodes 17 and 18 [see fig. 2 and col. 7, 45-46, 56-60].

Regarding claim 10, Onishi et al. teaches that a semiconductor comprising:

a substrate [consider the substrate formed by layers 4 and 5 in fig. 2];

a source area (7) formed in the substrate and having a doping of a first conductivity type (N+) [see fig. 2];

a drain area (1, 8) formed in the substrate and displaced from the source area (7) [see fig. 2], the drain area comprising:

a first drain portion (8) having a doping of the first conductivity type and a first doping concentration (N+), and

a second drain portion (1) having a doping of the first conductivity type and a second doping concentration (N) lower than the first doping concentration (N+) [see fig. 2], the second drain portion (1) being disposed between the first drain portion (8) and the source area (7) [see fig. 2];

a first region (2) formed in the second drain region (1), the first region having a doping of a second conductivity type (P-type) which is different than the first conductivity type [see fig. 2];

a second region (4) formed below the second drain region and having a doping of the first conductivity type (N-type) [see fig. 2]; and

a channel area (3) in the substrate between the source area and the drain area [see fig. 2].

Regarding claim 12, Onishi et al. teaches the second region (4) disposed substantially below the first region (2) in the substrate [see fig. 2].

Regarding claim 18, Onishi et al. teaches the first region (2) and the second region (4) form an area of dual implantation [see fig. 2 and col. 6, lines 64-66].

### ***Allowable Subject Matter***

7. Claims 3, 11 and 15-17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

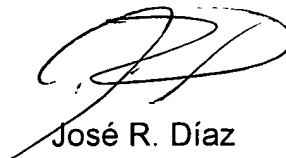
8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a drain area comprising a first drain portion, a second drain portion, a first region formed in the second drain portion, and a second region below the second drain portion; wherein the first and second drain portions and the second region have a first conductivity type, and the first region has a second conductivity type which is different to the first conductivity type; wherein the second drain portion has a doping concentration that is lower than the doping concentration of the first drain portion; and wherein the second region has a doping concentration higher than the second drain portion.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



José R. Díaz  
Examiner  
Art Unit 2815